

Abstract

A rectified analog input signal is compared with a threshold voltage by a voltage comparator, and counting direction of an up/down counter is switched based on the comparison result, and a latch circuit retains an output of the up/down counter, and then an analog-digital converting circuit converts an output of the latch signal into a direct-current voltage. In addition, two input terminals, to which a clock for up-count operation and a clock for down-count operation are independently provided, is provided in the up/down counter, and a timing pulse generating circuit for determining reset timing of the up/down counting circuit and latch timing of the latch circuit is provided.